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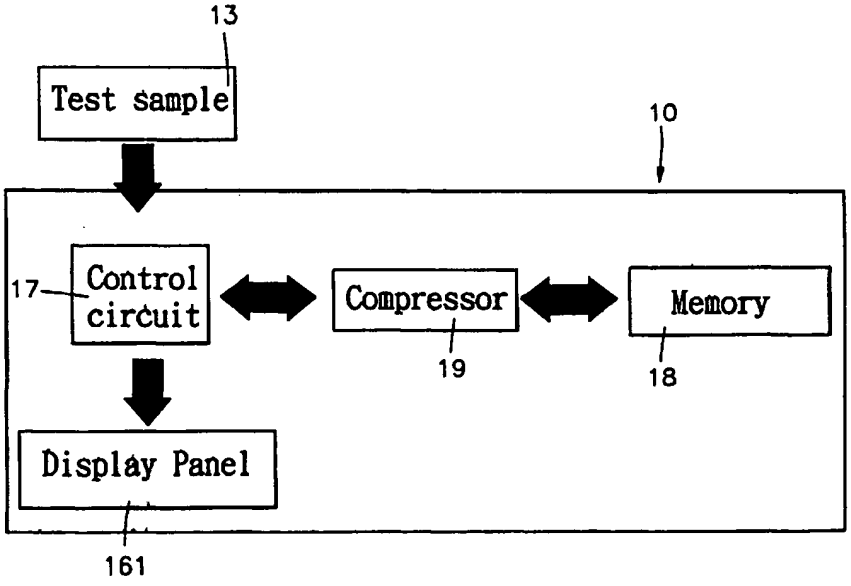
(54) Title: LOGIC ANALYZER DATA PROCESSING METHOD



(57) Abstract: A logic analyzer data processing method used in a logic analyzer (10) having a control circuit (17) adapted to read in test data from a test sample (13), a memory (18) controlled by the control circuit (17) to store the test data received from the test sample (13), and a display (161) adapted to display the test data fetched by the control circuit (17) from the memory (18), the method including the step of enabling the control circuit (17) to drive a compressor (19) to compress the test data received from the test sample (13) before storing it in the memory (18), and to depress the compressed test data before transmitting it from the memory (18) to the display (161).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

LOGIC ANALYZER DATA PROCESSING METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to logic analyzers and, more specifically, to logic analyzer data processing method, which decompresses test data obtained from test samples before storing in memory so that memory can store more test data.

2. Description of the Related Art:

FIG. 1 illustrates the arrangement of a logic data analyzer according to the prior art. The logic analyzer comprises a logic analyzer main unit **10'**. The logic analyzer main unit **10'** comprises detection devices **11'**. Each detection device **11'** has multiple lead-wires **111'** and a clip **113'** at the end of each lead-wire **111'** for fastening to a respective pin of the test sample (for example, digital circuit). The detection devices **11'** detect high/low potential status of every pin of the test sample at a fixed time interval, and then transmit test data to a computer **16'** through a transmission interface (for example, USB interface, LPT interface, or the like) **15**, enabling test data to be displayed on the display screen **161'** of the computer **16'**. FIG. 2 is a system block diagram of the prior art logic data analyzer. The logic analyzer main unit **10'** comprises a control circuit **17'** and a memory (for example, SRAM) **18'**. When received test data from the test sample **13'**, the control circuit **17'**

stores received test data in the memory 18'. When the memory space of the memory 18' used up, the control circuit 17' fetches storage test data from the memory 18', and then transmits fetched test data to the computer 16' through the transmission interface 15' for display on the display screen 161'of the computer 16'. Because the memory 18' has a limited data storage space, it may not be able to store a complete series of test data. When the user debugging the digital circuit (test sample) based on an incomplete test result, the debugging work may take much time, or may be unable to proceed.

Therefore, it is desirable to provide a logic analyzer data processing method that eliminates the aforesaid problem.

SUMMARY OF THE INVENTION

The present invention has been accomplished under the circumstances in view. It is therefore the main object of the present invention to provide a logic analyzer data processing method, which compresses the test data obtained from the test sample before storing it in the memory, so that the test data can be stored in less space in the memory.

According to one aspect of the present invention, the logic analyzer data processing method is used in a logic analyzer having a control circuit adapted to read in test data from a test sample, a memory controlled by the control circuit to store the test data received from the test sample, and a display adapted to display the

test data fetched by the control circuit from the memory, the method including the step of enabling the control circuit to drive a compressor to compress the test data before storing in the memory. According to another aspect of the present invention, the control circuit is controlled to drive the compressor to depress the compressed test data before transmitting it from the memory to the display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the arrangement of a logic analyzer according to the prior art.

FIG. 2 is a system block diagram of the logic data analyzer according to the prior art.

FIG. 3 is a system block diagram of a logic data analyzer according to the present invention.

FIG. 4 is an operational flow chart of the present invention.

FIG. 5 is a system block diagram of an alternate form of the logic data analyzer according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 3, the logic analyzer main unit, referenced by **10**, comprises a control circuit **17**, a memory **18** (for example SRAM), and a compressor **19**. When received the test data of the test sample **13**, for example, a digital circuit, the control circuit **17** transmits the received test data to the compressor **19**,

which compresses the test data to reduce its size, so that the compressed test data can be stored in less space in the memory **18**. When the memory space of the memory **18** used up (fully occupied by storage data), the control circuit **17** fetches the storage data from the memory **18**, and then directly transmits the fetched data to the computer **16** through the transmission interface **15** for display on the display panel **161** of the computer **16**. The control circuit **17** may control the compressor **19** to decompress the data fetched from the memory **18** before sending it to the computer **16**.

Referring to FIG. 4 and FIG. 3 again, the control circuit **17** works subject to the steps bellows:

(301) At first, read in the test data transmitted from the test sample **13** (the test data includes high/low potential status of every pin of the test sample **13** at a fixed time interval);

(302) Transmit the test data to the compressor **19**, and then drives the compressor **19** to compress the test data, so as to reduce the size of the test data;

(303) Store the compressed test data in the memory **18**;

(304) Determine if the memory space of the memory **18** has been used up (fully occupied) or not, and then proceed to step (305) if positive; or return to step (301) if negative;

(305) Fetch the compressed test data from the memory **18**, and then drive the compressor **19** to decompress the compressed

test data (the data decompression process may be eliminated);

(306) Transmit the fetched (or decompressed) test data through the transmission interface **15** to the computer **16** for display on the display panel **161** of the computer **16** for reference.

According to the aforesaid description, the test data obtained from the test sample is compressed to reduce the size, so that the compressed test data can be stored in less space in the memory **18**. Therefore, the memory **18** can store more test data.

FIG. 5 shows an alternate form of the present invention. According to this embodiment, the logic analyzer main unit **10** comprises a control circuit **17**, a memory **18** (for example SRAM), a compressor **19**, and a display panel **161**. When received the test data from the test sample **13**, the control circuit **17** transmits the received test data to the compressor **19**, which compresses the test data to reduce its size, so that the compressed test data can be stored in less space in the memory **18**. When the memory space of the memory **18** used up (fully occupied by storage data), the control circuit **17** fetches the storage data from the memory **18**, and then drives the compressor **19** to decompress the data fetched from the memory **18**, and then transmits the decompressed data to the display panel **161** for display.

A prototype of logic analyzer data processing method has

been constructed with the features of the annexed drawings of FIGS. 3~5. The logic analyzer data processing method functions smoothly to provide all of the features discussed earlier.

Although particular embodiments of the invention have been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.

What the invention claimed is:

1. A logic analyzer data processing method used in a logic analyzer, which comprises a control circuit adapted to read in test data from a test sample, a memory controlled by said control circuit to store the test data received from said test sample, and display means adapted to display the test data fetched by said control circuit from said memory, the method comprising the step of enabling said control circuit to drive a compressor to compress the test data received from said test sample before storing the test data in said memory.

2. The logic analyzer data processing method as claimed in claim 1, wherein said test sample is digital circuit.

3. The logic analyzer data processing method as claimed in claim 2, wherein the test data from said test sample includes high/low potential status of every pin of said test sample at a fixed time internal.

4. A logic analyzer data processing method used in a logic analyzer, which comprises a control circuit adapted to read in test data from a test sample, a memory controlled by said control circuit to store the test data received from said test sample, and display means adapted to display the test data fetched by said control circuit from said memory, the method comprising the step of enabling said control circuit to drive a compressor to compress the

test data received from said test sample before storing the test sample in said memory, and to depress the compressed test data before transmitting from said memory to said display means.

5. The logic analyzer data processing method as claimed in claim 4, wherein said test sample is a digital circuit.

6. The logic analyzer data processing method as claimed in claim 5, wherein the test data from said test sample includes high/low potential status of every pin of said test sample at a fixed time internal.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/31587

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 11/00
US CL : 714/39,25
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 714/39,25,30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,360,340 B1 (BROWN et al) 19 March 2002 (19.03.02), column 2, lines 30-67, column 5, lines 24-27	1-6
A	US 6,467,053 B1 (CONNOLLY et al) 15 October 2002 (15.10.02), abstract	1-3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 2002 (21.12.2002)	06 JAN 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Robert Beausoliel Telephone No. (703) 305-3900

Form PCT/ISA/210 (second sheet) (July 1998)

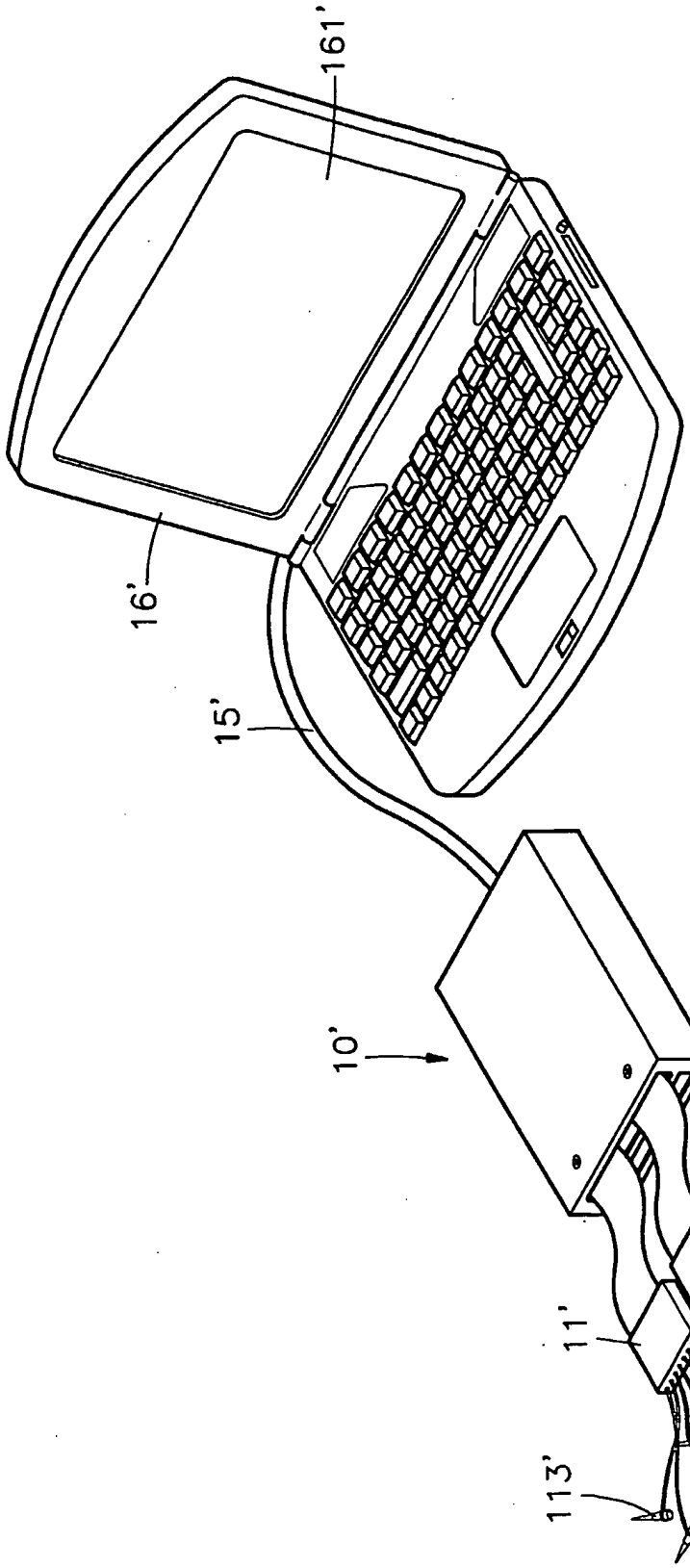

FIG. 1

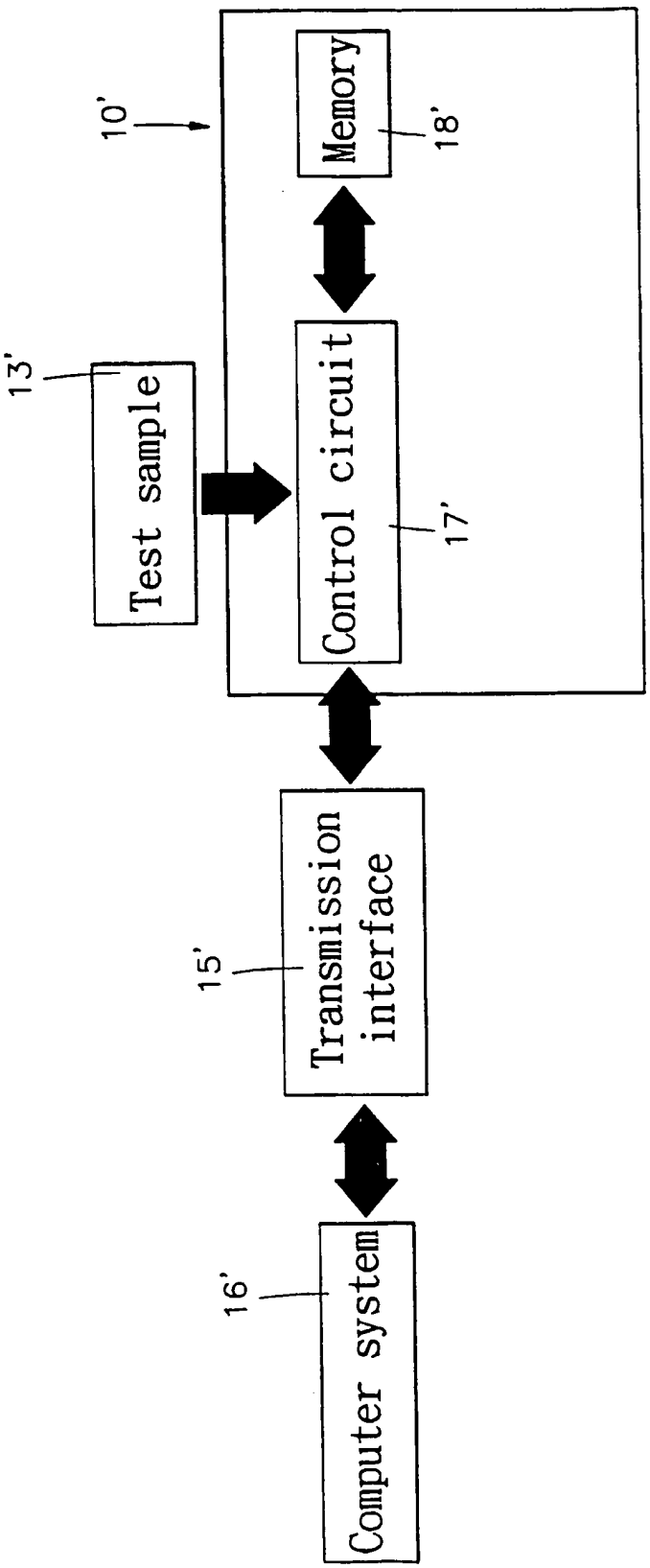
10'
Memory
18'
13'
Test sample
Control circuit
17'
15'
Transmission interface
16'
Computer system

FIG.2

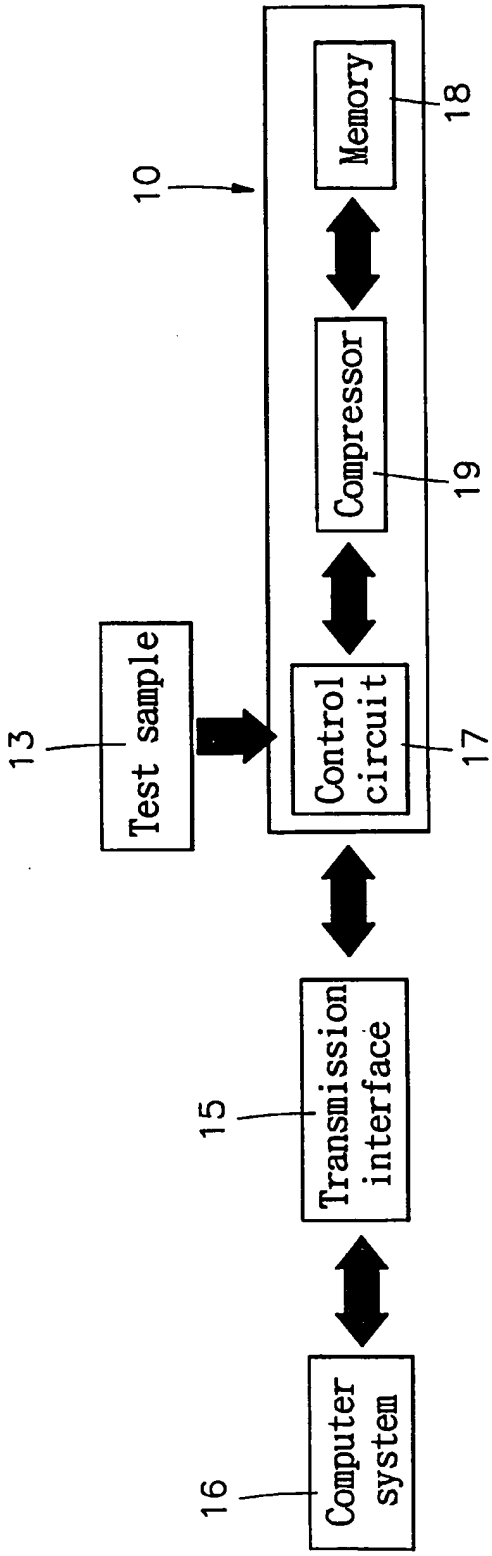
10
Memory
18
Compressor
19
Control circuit
17
13
Test sample
15
Transmission interface
16
Computer system

FIG.3

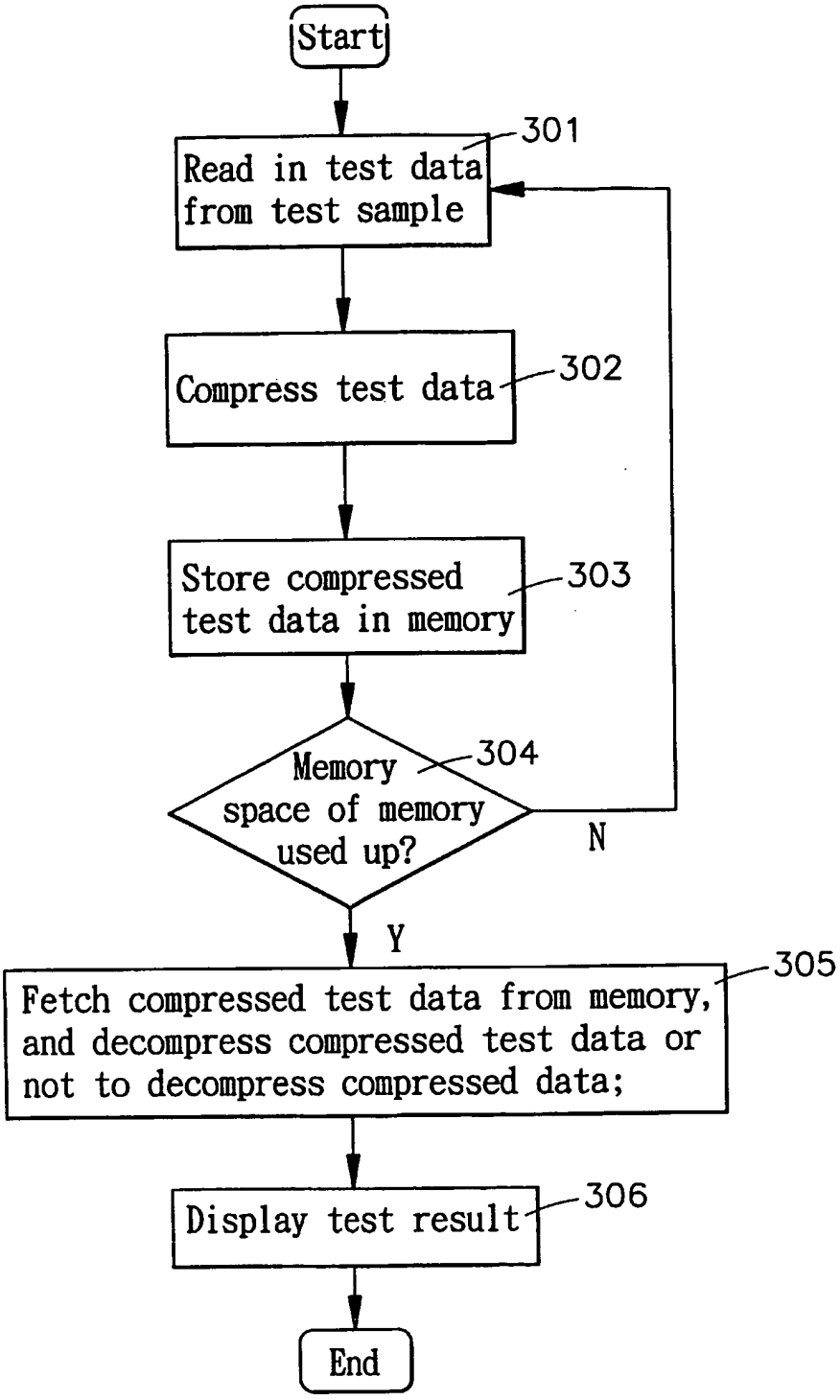
Start
Read in test data from test sample
301
Compress test data
302
Store compressed test data in memory
303
Memory space of memory used up?
304
N
Y
Fetch compressed test data from memory, and decompress compressed test data or not to decompress compressed data;
305
Display test result
306
End

FIG. 4

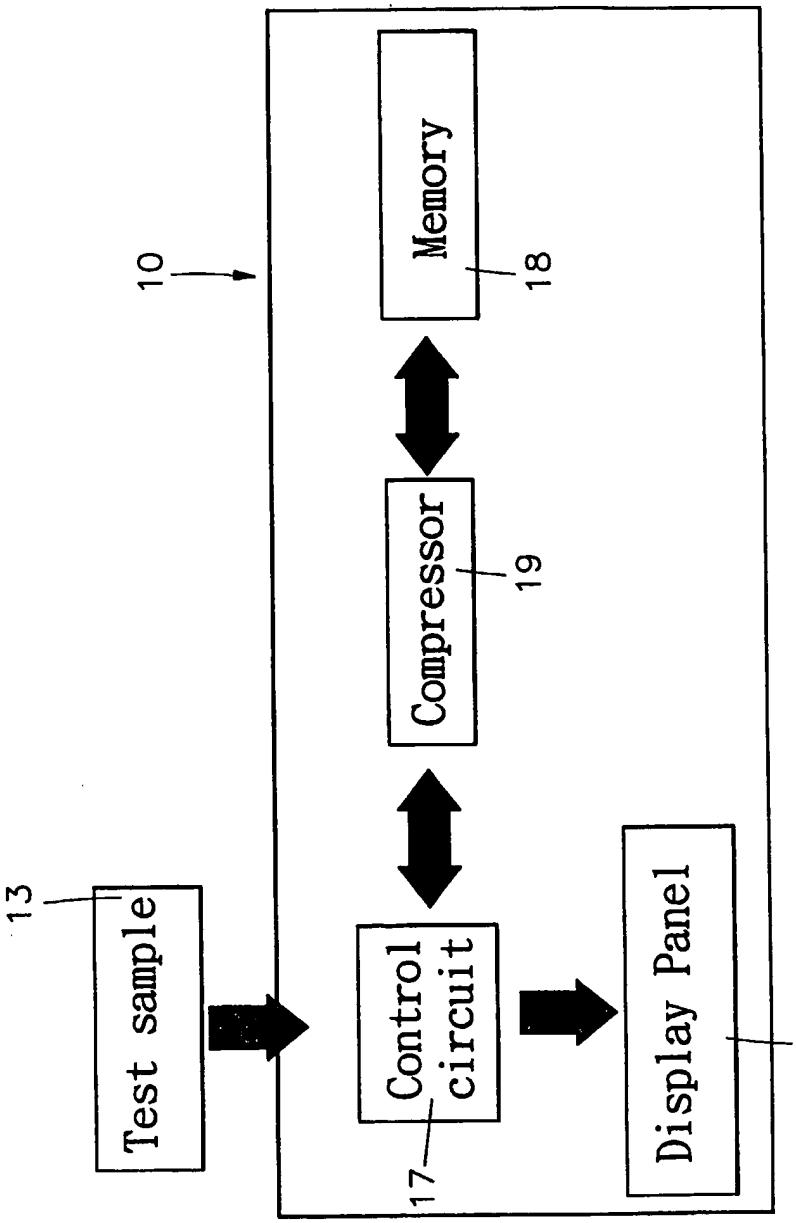
10
Memory
18
Compressor
19
Control circuit
17
Test sample
13
Display Panel
161

FIG.5